

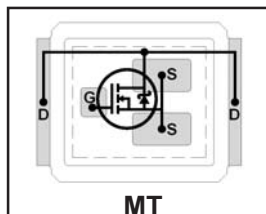
# IRF6691PbF

# IRF6691TRPbF

DirectFET™ Power MOSFET ②

Typical values (unless otherwise specified)

$V_{DS}$	$V_{GS}$	$R_{DS(on)}$	$R_{DS(on)}$		
20V max	±12V max	1.2mΩ @ 10V	1.8mΩ @ 4.5V		
$Q_{g\ tot}$	$Q_{gd}$	$Q_{gs2}$	$Q_{rr}$	$Q_{oss}$	$V_{gs(th)}$
47nC	15nC	4.4nC	26nC	30nC	2.0V



- RoHs Compliant ①
- Lead-Free (Qualified up to 260°C Reflow)
- Application Specific MOSFETs
- Ideal for CPU Core DC-DC Converters
- Low Conduction Losses
- High Cdv/dt Immunity
- Low Profile (<0.7mm)
- Dual Sided Cooling Compatible ①
- Compatible with existing Surface Mount Techniques ①

Applicable DirectFET Outline and Substrate Outline (see p.7,8 for details)①

SQ	SX	ST		MQ	MX	<b>MT</b>			
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## Description

The IRF6691PbF combines the latest HEXFET® Power MOSFET Silicon technology with the advanced DirectFET™ packaging to achieve the lowest on-state resistance in a package that has the footprint of a SO-8 and only 0.7 mm profile. The DirectFET package is compatible with existing layout geometries used in power applications, PCB assembly equipment and vapor phase, infra-red or convection soldering techniques. Application note AN-1035 is followed regarding the manufacturing methods and processes. The DirectFET package allows dual sided cooling to maximize thermal transfer in power systems, improving previous best thermal resistance by 80%.

The IRF6691PbF balances industry leading on-state resistance while minimizing gate charge along with ultra low package inductance to reduce both conduction and switching losses. This part contains an integrated Schottky diode to reduce the Qrr of the body drain diode further reducing the losses in a Synchronous Buck circuit. The reduced losses make this product ideal for high frequency/high efficiency DC-DC converters that power high current loads such as the latest generation of microprocessors. The IRF6691PbF has been optimized for parameters that are critical in synchronous buck converter's SyncFET sockets.

## Absolute Maximum Ratings

	Parameter	Max.	Units
$V_{DS}$	Drain-to-Source Voltage	20	V
$V_{GS}$	Gate-to-Source Voltage	±12	
$I_D @ T_A = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ ③	32	A
$I_D @ T_A = 70^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ ③	26	
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ ④	180 ⑤	
$I_{DM}$	Pulsed Drain Current ⑤	260	
$E_{AS}$	Single Pulse Avalanche Energy ⑥	230	mJ
$I_{AR}$	Avalanche Current ⑤	26	A

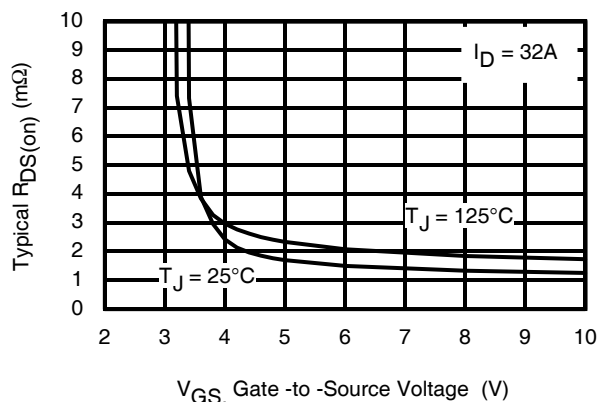


Fig 1. Typical On-Resistance vs. Gate-to-Source Voltage

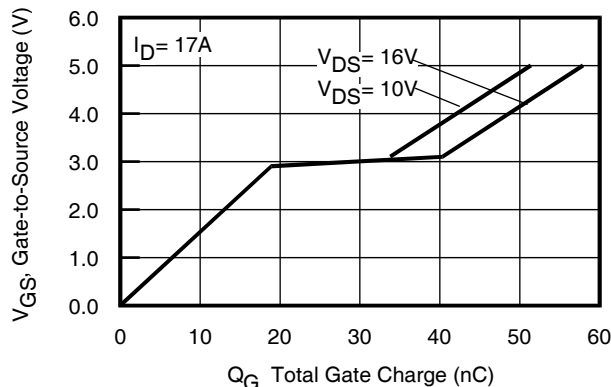


Fig 2. Total Gate Charge vs. Gate-to-Source Voltage

Notes:

- ① Click on this section to link to the appropriate technical paper.
- ② Click on this section to link to the DirectFET Website.
- ③ Surface mounted on 1 in. square Cu board, steady state.

- ④  $T_C$  measured with thermocouple mounted to top (Drain) of part.
- ⑤ Repetitive rating; pulse width limited by max. junction temperature.
- ⑥ Starting  $T_J = 25^\circ C$ ,  $L = 0.72mH$ ,  $R_G = 25\Omega$ ,  $I_{AS} = 26A$ .

## Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$BV_{DSS}$	Drain-to-Source Breakdown Voltage	20	—	—	V	$V_{GS} = 0V, I_D = 1.0mA$
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	12	—	mV/°C	Reference to $25^\circ\text{C}, I_D = 10mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	1.8	2.5	m $\Omega$	$V_{GS} = 4.5V, I_D = 12A$ ⑦
		—	1.2	1.8		$V_{GS} = 10V, I_D = 15A$ ⑦
$V_{GS(th)}$	Gate Threshold Voltage	1.6	—	2.5	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-4.1	—	mV/°C	$I_D = 10mA$ , reference to $25^\circ\text{C}$
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	1.4	mA	$V_{DS} = 20V, V_{GS} = 0V$
		—	—	500	$\mu A$	$V_{DS} = 16V, V_{GS} = 0V$
		—	—	5	mA	$V_{DS} = 16V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 12V$
	Gate-to-Source Reverse Leakage	—	—	-100	nA	$V_{GS} = -12V$
$g_{fs}$	Forward Transconductance	110	—	—	S	$V_{DS} = 10V, I_D = 26A$
$Q_g$	Total Gate Charge	—	47	71	nC	$V_{DS} = 10V$ $V_{GS} = 4.5V$ $I_D = 17A$ See Fig. 14
$Q_{gs1}$	Pre-V <sub>th</sub> Gate-to-Source Charge	—	14	—		
$Q_{gs2}$	Post-V <sub>th</sub> Gate-to-Source Charge	—	4.4	—		
$Q_{gd}$	Gate-to-Drain Charge	—	15	—		
$Q_{godr}$	Gate Charge Overdrive	—	14	—		
$Q_{sw}$	Switch Charge ( $Q_{gs2} + Q_{gd}$ )	—	19	—	nC	
$Q_{oss}$	Output Charge	—	30	—	nC	$V_{DS} = 10V, V_{GS} = 0V$
$R_G$	Gate Resistance	—	0.60	1.5	$\Omega$	
$t_{d(on)}$	Turn-On Delay Time	—	23	—	ns	$V_{DD} = 16V, V_{GS} = 4.5V$ ⑦ $I_D = 26A$ Clamped Inductive Load See Fig. 15 & 16
$t_r$	Rise Time	—	95	—		
$t_{d(off)}$	Turn-Off Delay Time	—	25	—		
$t_f$	Fall Time	—	10	—		
$C_{iss}$	Input Capacitance	—	6580	—	pF	$V_{GS} = 0V$ $V_{DS} = 10V$ $f = 1.0MHz$
$C_{oss}$	Output Capacitance	—	2070	—		
$C_{rss}$	Reverse Transfer Capacitance	—	840	—		

## Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	200 <sup>⑧</sup>	A	MOSFET symbol showing the integral reverse p-n junction diode.
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	260		
$V_{SD}$	Diode Forward Voltage	—	—	0.65	V	$T_J = 25^\circ\text{C}, I_S = 25A, V_{GS} = 0V$ ⑦
$t_{rr}$	Reverse Recovery Time	—	32	48	ns	$T_J = 25^\circ\text{C}, I_F = 25A$
$Q_{rr}$	Reverse Recovery Charge	—	26	39	nC	$di/dt = 100A/\mu s$ ⑦ See Fig. 17

### Notes:

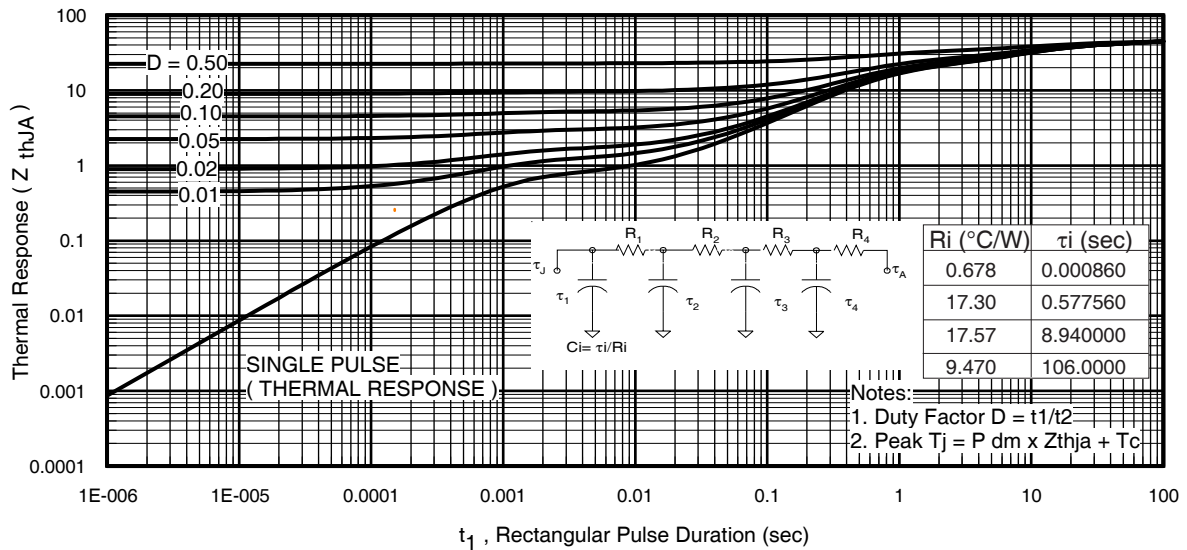
- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Pulse width  $\leq 400\mu s$ ; duty cycle  $\leq 2\%$ .
- ③ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 150A.

**Absolute Maximum Ratings**

$P_D @ T_A = 25^\circ\text{C}$	Power Dissipation ③	2.8	W
$P_D @ T_A = 70^\circ\text{C}$	Power Dissipation ③	1.8	
$P_D @ T_C = 25^\circ\text{C}$	Power Dissipation ④	89	
$T_P$	Peak Soldering Temperature	270	°C
$T_J$	Operating Junction and	-40 to + 150	
$T_{STG}$	Storage Temperature Range		

**Thermal Resistance**

	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient ③ ①	---	45	°C/W
$R_{\theta JA}$	Junction-to-Ambient ⑨ ①	12.5	---	
$R_{\theta JA}$	Junction-to-Ambient ⑩ ①	20	---	
$R_{\theta JC}$	Junction-to-Case ④ ①	---	1.4	
$R_{\theta J-PCB}$	Junction-to-PCB Mounted	1.0	---	
	Linear Derating Factor ③	0.022		W/°C



**Fig 3.** Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

**Notes:**

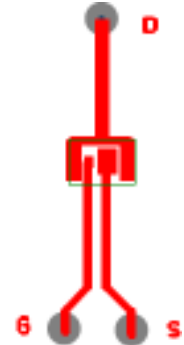
- ③ Used double sided cooling, mounting pad.
- ④ Mounted on minimum footprint full size board with metalized back and with small clip heatsink.
- ①  $R_{\theta}$  is measured at  $T_J$  of approximately  $90^\circ\text{C}$ .



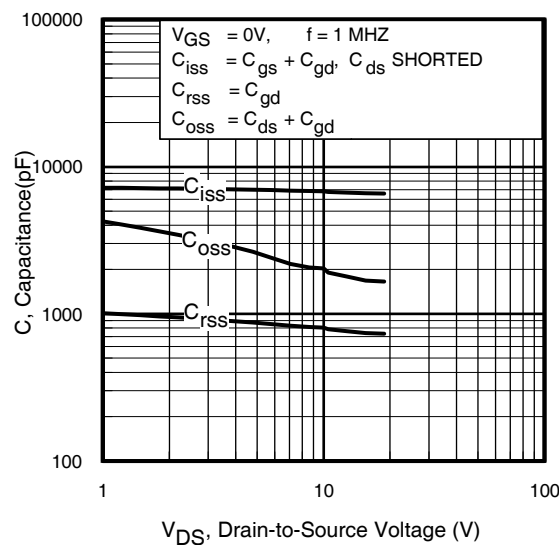
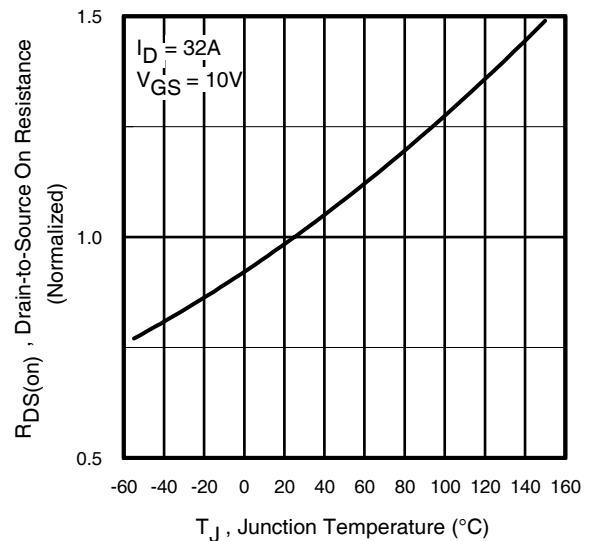
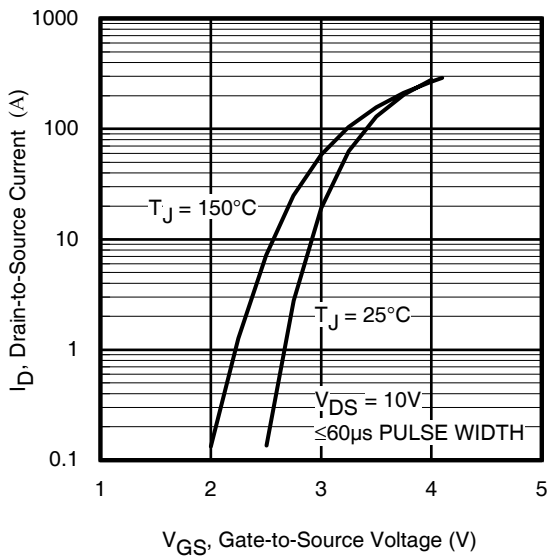
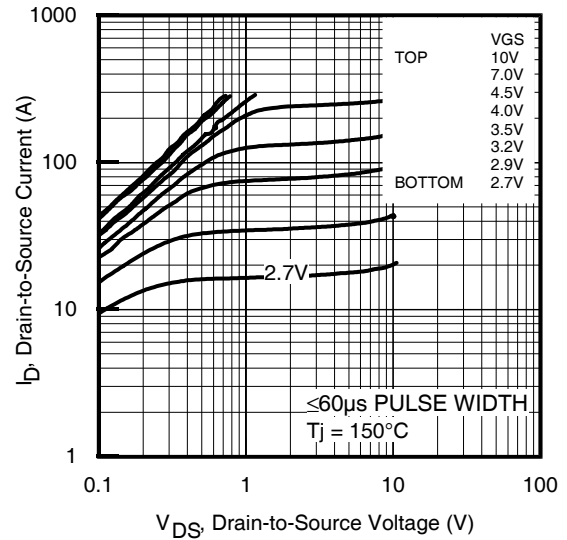
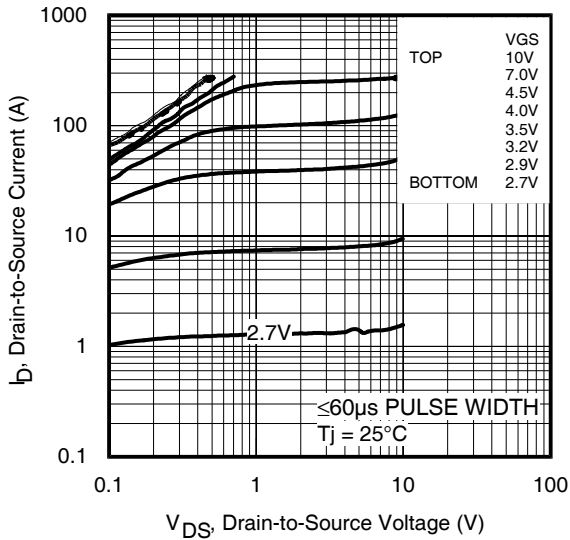
③ Surface mounted on 1 in. square Cu (still air).



④ Mounted to a PCB with small clip heatsink (still air)



⑩ Mounted on minimum footprint full size board with metalized back and with small clip heatsink (still air)



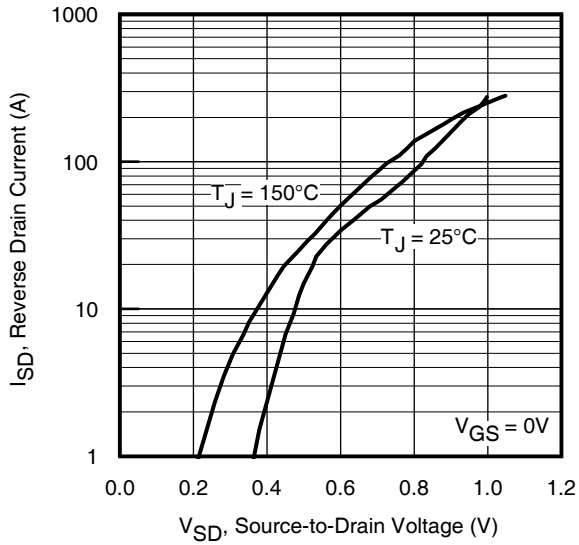


Fig 9. Typical Source-Drain Diode Forward Voltage

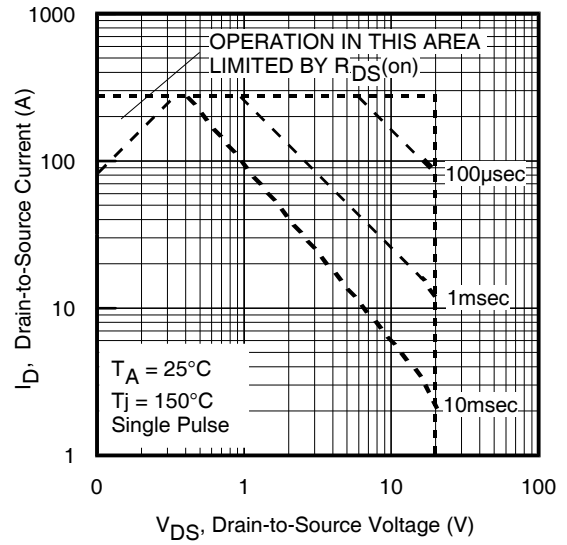


Fig10. Maximum Safe Operating Area

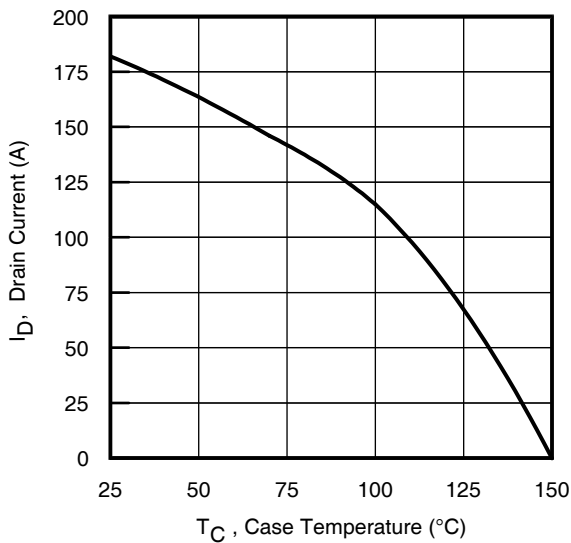


Fig 11. Maximum Drain Current vs. Case Temperature

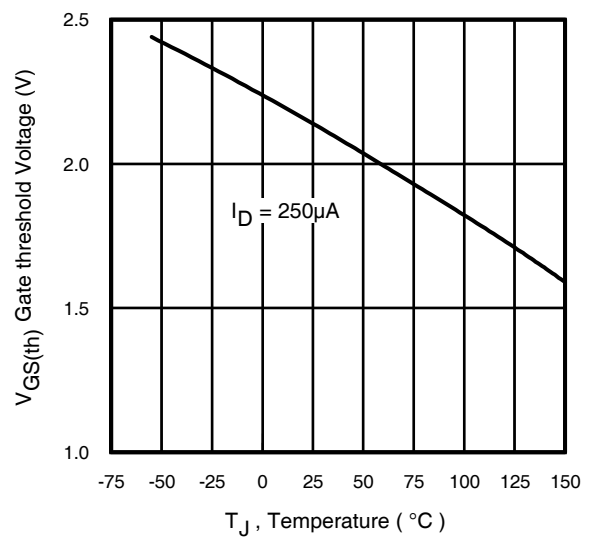


Fig 12. Threshold Voltage vs. Temperature

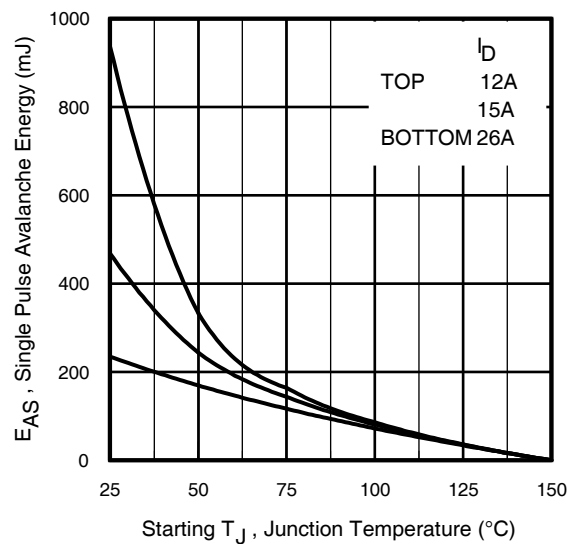
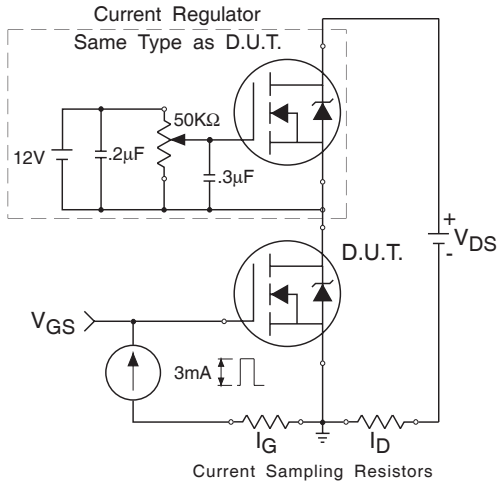
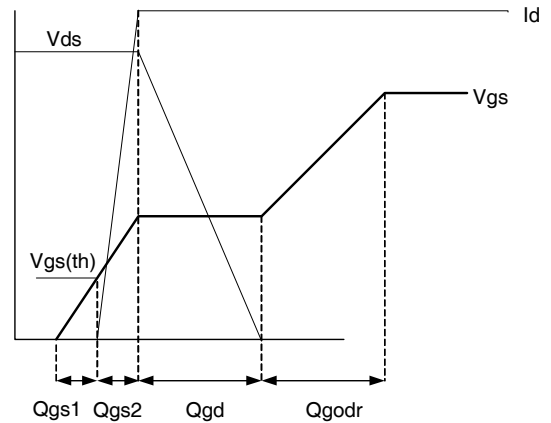


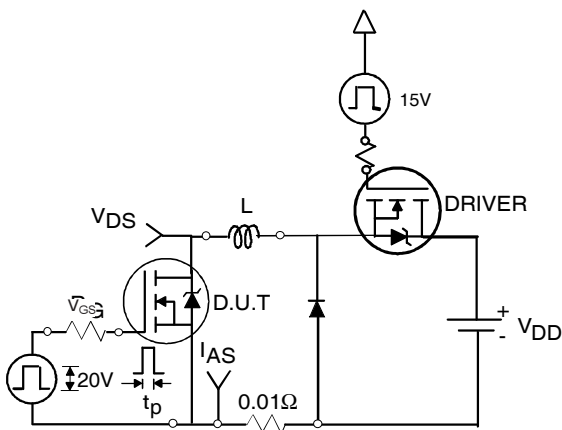
Fig 13. Maximum Avalanche Energy vs. Drain Current



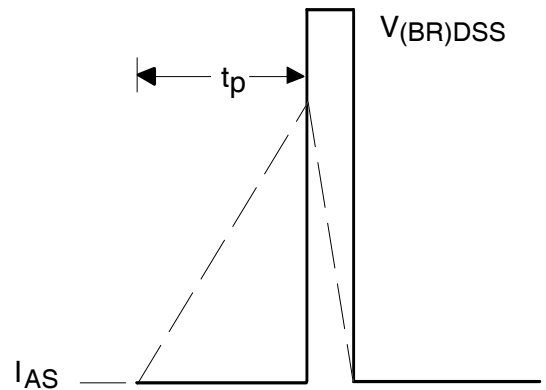
**Fig 14a.** Gate Charge Test Circuit



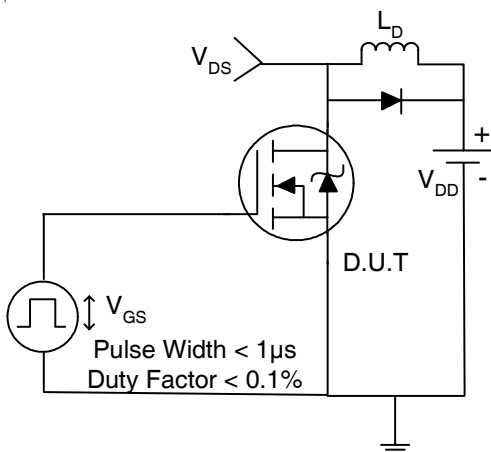
**Fig 14b.** Gate Charge Waveform



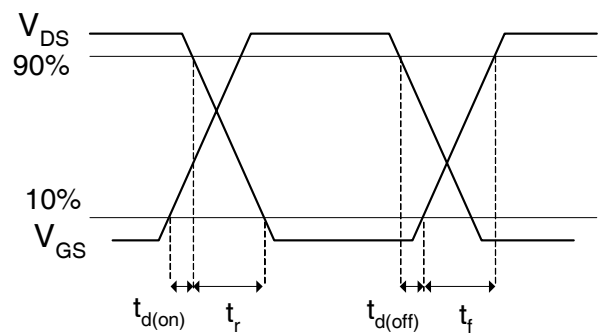
**Fig 15a.** Unclamped Inductive Test Circuit



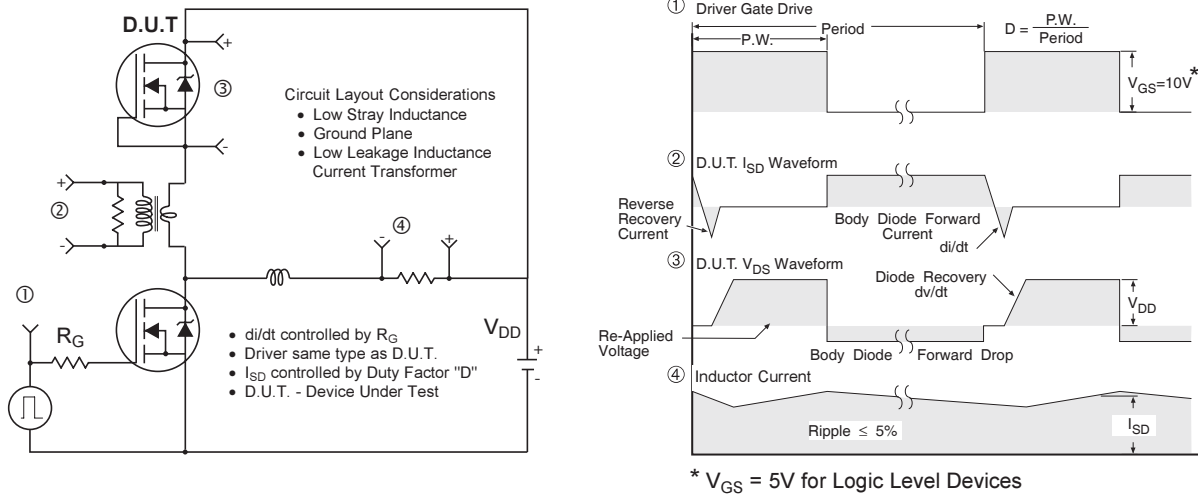
**Fig 15b.** Unclamped Inductive Waveforms



**Fig 16a.** Switching Time Test Circuit



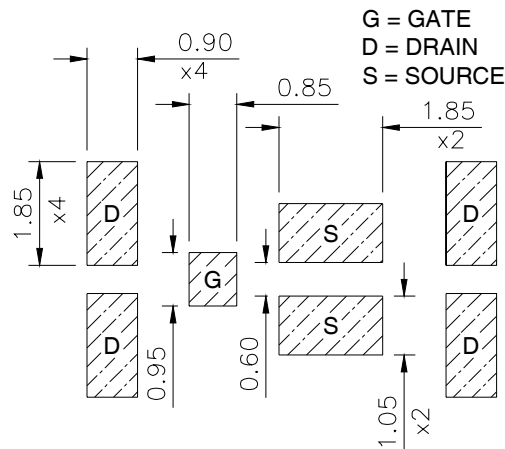
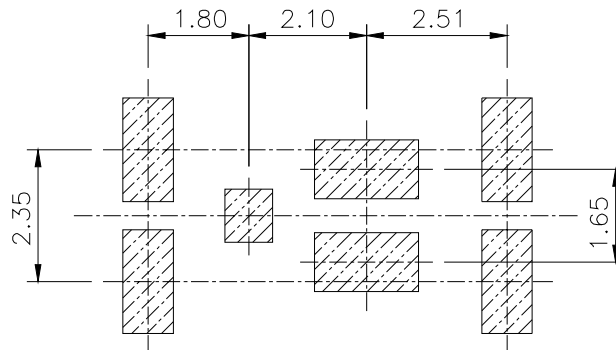
**Fig 16b.** Switching Time Waveforms



**Fig 17.** Diode Reverse Recovery Test Circuit for N-Channel HEXFET® Power MOSFETs

**DirectFET™ Board Footprint, MT Outline ③ (Medium Size Can, T-Designation).**

Please see DirectFET application note AN-1035 for all details regarding the assembly of DirectFET. This includes all recommendations for stencil and substrate designs.



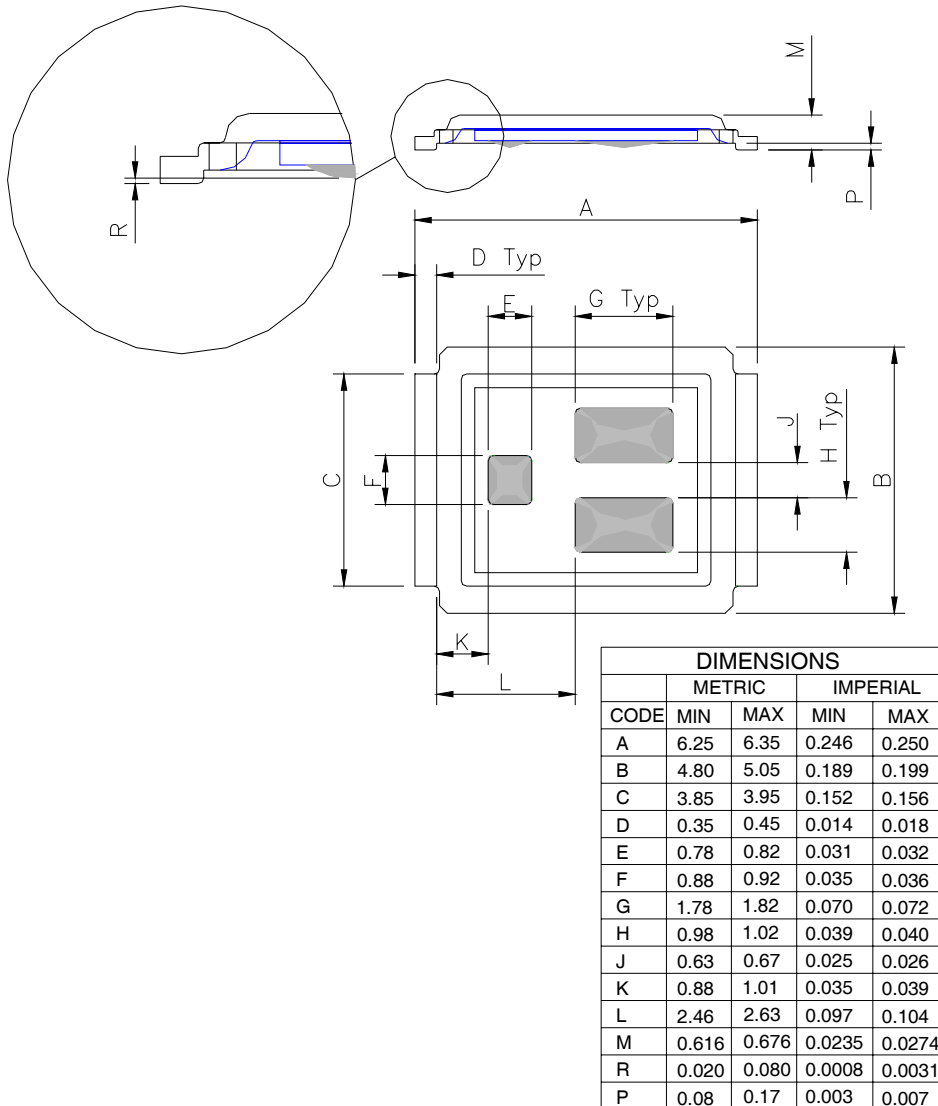
# IRF6691PbF

PROVISIONAL

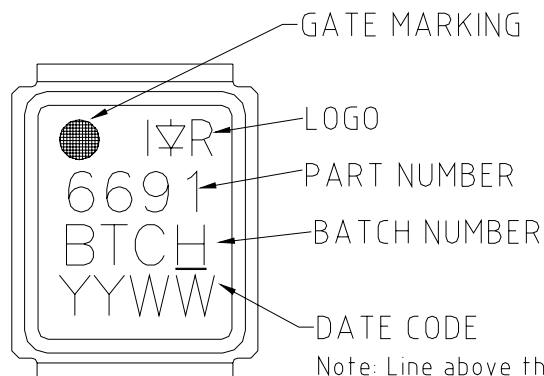
International  
**IR** Rectifier

## DirectFET™ Outline Dimension, MT Outline (Medium Size Can, T-Designation).

Please see DirectFET application note AN-1035 for all details regarding the assembly of DirectFET. This includes all recommendations for stencil and substrate designs.



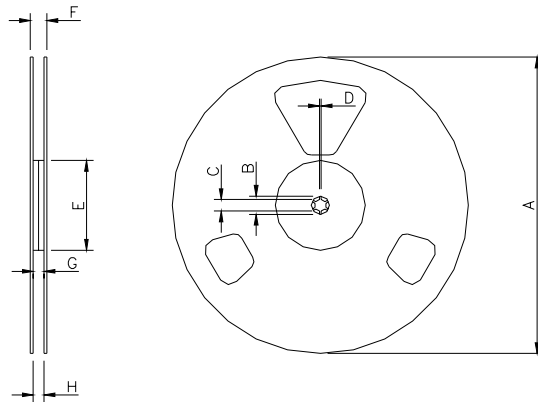
## DirectFET™ Part Marking



Note: Line above the last character of the date-code indicates "Lead-Free".

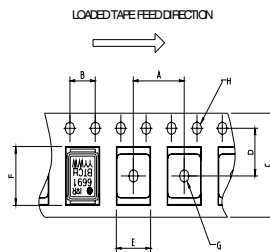


DirectFET™ Tape & Reel Dimension (Showing component orientation).



NOTE: Controlling dimensions in mm  
 Std reel quantity is 4800 parts. (ordered as IRF6691TRPBF). For 1000 parts on 7" reel, order IRF6691TR1PBF

REEL DIMENSIONS								
CODE	STANDARD OPTION (QTY 4800)				TR1 OPTION (QTY 1000)			
	METRIC		IMPERIAL		METRIC		IMPERIAL	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	330.0	N.C	12.992	N.C	177.77	N.C	6.9	N.C
B	20.2	N.C	0.795	N.C	19.06	N.C	0.75	N.C
C	12.8	13.2	0.504	0.520	13.5	12.8	0.53	0.50
D	1.5	N.C	0.059	N.C	1.5	N.C	0.059	N.C
E	100.0	N.C	3.937	N.C	58.72	N.C	2.31	N.C
F	N.C	18.4	N.C	0.724	N.C	13.50	N.C	0.53
G	12.4	14.4	0.488	0.567	11.9	12.01	0.47	N.C
H	11.9	15.4	0.469	0.606	11.9	12.01	0.47	N.C



NOTE: CONTROLLING DIMENSIONS IN MM

CODE	DIMENSIONS			
	METRIC		IMPERIAL	
	MIN	MAX	MIN	MAX
A	790	810	0.311	0.320
B	390	410	0.154	0.161
C	11.90	12.30	0.469	0.494
D	5.45	5.55	0.215	0.219
E	5.10	5.30	0.201	0.209
F	6.50	6.70	0.256	0.264
G	1.50	N.C	0.059	N.C
H	1.50	1.60	0.059	0.063

Data and specifications subject to change without notice.  
 This product has been designed and qualified for the Consumer market.  
 Qualification Standards can be found on IR's Web site.

Note: For the most current drawings please refer to the IR website at:  
<http://www.irf.com/package/>